What is claimed :

1. A flash memory device comprising:

a plurality of sets of adjacent local bit lines;

a plurality of global bit lines; and

a plurality of select transistors each having a control gate, each select transistor is coupled between one of the local bit lines in each set of local bit lines and one of the global bit lines, wherein each local bit line in each set of local bit lines is coupled to a different global bit line.

2. The flash memory device of claim 1 further comprising:

a plurality of select lines to activate the control gates on the select transistors, each select line is coupled to the control gates on associated select transistors, wherein the associated select transistors are select transistors that are coupled to the local bit lines in an associated set of local bit lines.

3. The flash memory device of claim 1 wherein each set of local bit lines comprises two or more local bit lines.

4. The flash memory device of claim 1 wherein each set of local bit lines contains an even number of bit lines.

5. A flash memory device comprising:

a plurality of sets of adjacent local bit lines;

a plurality of global bit lines; and

a plurality of select transistors each having a control gate, the plurality of select transistors are coupled between the plurality of sets of adjacent local bit lines and the plurality of global bit lines, wherein every other local bit line in one of the plurality of sets of local bit lines is coupled to a different one of the plurality of global bit lines.

6. The flash memory device of claim 5 further comprising:

a plurality of select lines to activate the control gates on the select transistors, each select line is coupled to the control gates on associated select transistors, wherein the associated select transistors are select transistors that are coupled to every other global bit line.

7. The flash memory device of claim 5 wherein each set of local bit lines comprises four local bit lines.

8. The flash memory device of claim 5 wherein the plurality of global bit lines comprises two global bit lines.

9. The flash memory device of claim 5 wherein the local bit lines in a set of local bit lines comprise a first, second, third and fourth local bit line, further wherein the plurality of global bit lines comprise a first and a second global bit line, the flash memory device further comprises:

the first global bit line coupled to the first and third local bit lines; and

the second global bit line coupled to the second and fourth local bit lines.

10. The flash memory device of claim 9 further comprising:

a first select line coupled to control gates of select transistors coupled to the first and second local bit lines; and

a second select line coupled to control gates of select transistors coupled to the third and fourth local bit lines.

11. A flash memory device comprising:

a plurality of local bit lines positioned generally parallel with each other;

a plurality of select transistors coupled to an associated one of the plurality of local bit lines; and

a plurality of global bit lines, each global bit line is coupled to a pair of associated select transistors, wherein the pair of select transistors are coupled to alternate local bit lines.

12. The flash memory device of claim 11 wherein the plurality of local bit lines comprise a first local bit line, a second local bit line, a third local bit and a fourth local bit line, wherein the flash memory device further comprises:

a first select line coupled to control gates of the select transistors coupled to the first and second local bit lines; and

a second select line coupled to control gates of the select transistors coupled to the third and fourth local bit lines.

13. The flash memory device of claim 11 wherein the device is manufactured so the local bit lines are on a different planer level than the global bit lines.

14. The flash memory device of claim 13 wherein the local bit lines are formed on a first metal level and the global bit lines are formed on a second metal level.

15. A flash memory system comprising:

an array of flash memory cells arranged in rows and columns;

a plurality of local bit lines positioned generally parallel with each other, each local bit line is coupled to an associated column of the memory array;

a plurality of global bit lines; and

a select circuit to selectively couple the local bit lines to the global bit lines, wherein every other local bit line is coupled to a different global bit line.

16. The flash memory system of claim 15 wherein the plurality of local bit lines comprise a first local bit line, a second local bit line, a third local bit and a fourth local bit line.

17. The flash memory system of claim 15 wherein the select circuit comprises a select transistor coupled to each of the plurality of bit lines.

18. The flash memory system of claim 17 further comprising:

a first select line to activate select transistors coupled to the first and second local bit lines; and

a second select line to activate select transistors coupled to the third and fourth local bit lines.

19. A flash memory system comprising:

an array of flash memory cells arranged in rows and columns;

four local bit lines positioned generally parallel with each other;

a pair of global bit lines, each global bit line is selectively coupled to a pair of the four local bit lines, wherein the pair of local bit lines are alternately positioned with respect to each other; and

a multiplex circuit to selectively couple the associated local bit lines to the associated global bit lines.

20. The flash memory system of claim 19 wherein the multiplex circuit comprises:

four select transistors coupled between an associated local bit line and an associated global bit line, each select transistor having a control gate.

21. The flash memory system of claim 20 further comprising:

a first select line coupled to control gates of the select transistors that are coupled to a first and a second local bit line of the four local bit lines; and

a second select line coupled to control gates of the select transistors that are coupled to a third and a fourth local bit line of the four local bit lines.

22. The flash memory system of claim 19 wherein the array of flash memory cells are positioned adjacent the multiplex circuit.

23. A flash memory system comprising:

an array of flash memory cells arranged in rows and columns;

four local bit lines positioned generally parallel with each other;

a first and a second global bit line; and

a first multiplex circuit to selectively couple a first pair of the four local bit lines with the first global bit line, wherein the first pair of local bit lines are separated by one of the four local bit lines; and

a second multiplex circuit to selectively couple a second pair of the four local bit lines to the second global bit line.

24. The flash memory system of claim 23 wherein:

the first multiplex circuit comprises first and second select transistors, the first select transistor is coupled between a first local bit line of the four local bit lines and the first global bit line, the second select transistor is coupled between a third local bit line of the four local bit lines and the second global bit line; and

the second multiplex circuit comprises third and fourth select transistors, the third select transistor is coupled between a second local bit line of the four local bit lines and an the second global bit line, the fourth select transistor is coupled between a fourth local bit line of the four local bit lines and the second global bit line.

25. The flash memory system of claim 24 further comprising:

a first select line coupled to control gates of the first and second select transistors; and

a second select line coupled to control gates of the third and fourth select transistors.

26. The flash memory system of claim 23 wherein the array of flash memory cells is positioned between the first multiplex circuit and the second multiplex circuit.

27. A flash memory system comprising:

an array of flash memory cells arranged in rows and columns;

a first local bit line coupled to an associated first column of flash memory cells;

a second local bit line coupled to an associated second column of flash memory cells;

a third local bit line coupled to an associated third column of flash memory cells;

a fourth local bit line coupled to an associated fourth column of flash memory cells, wherein the first, second, third and fourth local bit lines are positioned generally parallel with each other;

a first global bit line;

a second global bit line;

first, second, third and fourth select transistors, the first select transistor is coupled to the first local bit line and the first global bit line, the second select transistor is coupled to the second local bit line and the second global bit line, the third select transistor is coupled to the third local bit line and the first global bit line, the fourth select transistor is coupled to the fourth local bit line and the second global bit line;

a first select line to activate the first and second select transistors; and

a second select line to activate the third and fourth select transistors.

28. The flash memory system of claim 27 wherein the first and third select transistors are located at opposite ends of the array from the second and fourth select transistors.

29. The flash memory device of claim 27 wherein the local bit lines are formed on a first metal level and the global bit lines are formed on a second metal level.

30. An integrated select circuit comprising:

a first drain diffusion region;

a second drain diffusion region laterally spaced apart from the first drain diffusion region;

a source diffusion region laterally spaced between the first drain diffusion region and the second drain diffusion region;

a first local bit line coupled to the first drain diffusion region;

a second local bit line coupled to the second drain diffusion region; and

a global bit line coupled to the source diffusion region, wherein the first drain diffusion region is laterally wider than the second drain diffusion region such that a third local bit line can traverse between the first local bit line and the second local bit line.

31. The integrated select circuit of claim 30 wherein the third local bit line is generally located above the first drain diffusion region.

32. The integrated select circuit of claim 30 further comprising:

a first gate positioned between the first drain diffusion region and the source diffusion region, the first gate is coupled to a select line; and

a second gate positioned between the source diffusion region and the second drain diffusion region, the second gate is coupled another select line.

33. The integrated select circuit of claim 30 wherein the device is manufactured so the local bit lines are on a different planer level than the global bit lines.

34. The integrated select circuit of claim 33 wherein the local bit lines are formed on a first metal level and the global bit lines are formed on a second metal level.

35. A memory device comprising:

an array of memory cells coupled to even and odd local bit lines; and

select transistors to couple the even local bit lines to even global bit lines and to couple the odd local bit lines to odd global bit lines.

36. The memory device of claim 35, wherein the local bit lines are positioned approximately parallel with each other and are sequentially numbered, further wherein the global bit lines are positioned approximately parallel with each other and are sequentially numbered.

37. The memory device of claim 35, further comprising:

a first multiplexer circuit including some of the select transistors; and

a second multiplexer circuit including the remaining select transistors, wherein the array of memory is positioned between the first and second multiplexer circuits.

38. A method of forming an integrated circuit comprising:

selectively coupling select transistors between a local bit line in a set of local bit lines and an associated global bit line, wherein each local bit line in the set of local bit lines is coupled to a different global bit line; and

selectively coupling a select line to control gates of the select transistors coupled to the local bit lines in a set of local bit lines.

39. The method of claim 37, wherein each set of local bit lines contains an even number of bit lines.

40. A method of operating a flash memory comprising:

programming a memory array with an alternate bit line program;

monitoring the logic states in global bit lines in response to the alternate bit line stress program;

comparing the pattern of logic states in global bit lines with a predetermined pattern; and

locating local and global bit line shorts in response to the monitoring.

41. The method of claim 40 wherein all global line shorts are detected by use of the single alternate bit line program.

42. The method of claim 40 wherein programming the memory array with alternate bit line program comprises:

programming even columns of addresses of a memory array to a first logic state; and

programming odd columns of addresses of a memory array to an opposite logic state.

43. The method of claim 42 wherein the predetermined pattern of logic states comprises alternating "High," "Low" states.

44. A method of operating a flash memory comprising:

programming even columns of addresses of a memory array to a first logic state;

programming odd columns of addresses of a memory array to an opposite logic state;

monitoring the output of the memory array; and

detecting local bit line shorts and all global bit lines shorts in response to a pattern of logic states in the global bit lines.

45. The method of claim 44 wherein any output of the memory array not comprising a series of alternating states indicates a short in either a local or global bit line.

46. The method of claim 44 wherein monitoring the output of the memory array comprises monitoring the state of global bit lines.

47. A method of operating a memory system comprising:

programming even columns of addresses of a memory array to a first logic state;

programming odd columns of addresses of a memory array to an opposite logic state;

monitoring logic states in global bit lines; and

simultaneously determining short circuits in local and global bit lines in response to a pattern of logic states in the global bit lines.

48. A method of operating an integrated circuit memory comprising:

selectively coupling odd local bit lines to odd global bit lines; and

selectively coupling even local bit lines to even global bit lines.

49. The method of claim 48 wherein select transistors are coupled between the local bit lines and the global bit lines.

50. A method of conducting an alternative bit line stress on a flash memory comprising:

applying activation signals to select transistors to selectively couple global bit lines to associated local bit lines, wherein adjacent local bit lines are selectively coupled to different global bit lines; and

applying potential voltage differences across adjacent global bit lines.

51. The method of claim 50, wherein resulting voltage potentials across adjacent local bit lines are different.

52. A method of conducting an alternative bit line stress on a flash memory comprising:

selectively coupling a first local bit line to a first global bit line;

selectively coupling a second local bit line to a second global bit line;

selectively coupling a third local bit line to the first global bit line;

selectively coupling a fourth local bit line to the second global bit line; and

applying a voltage potential across the first and second global bit lines.

53. The method of claim 52, wherein there is a voltage potential difference across adjacent local bit lines as the result of applying the voltage potential across the first and second global bit lines.

54. The method of claim 52, wherein the local bit lines are sequentially positioned adjacent each other.

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